

Component Creation: Quartus Tool Tip

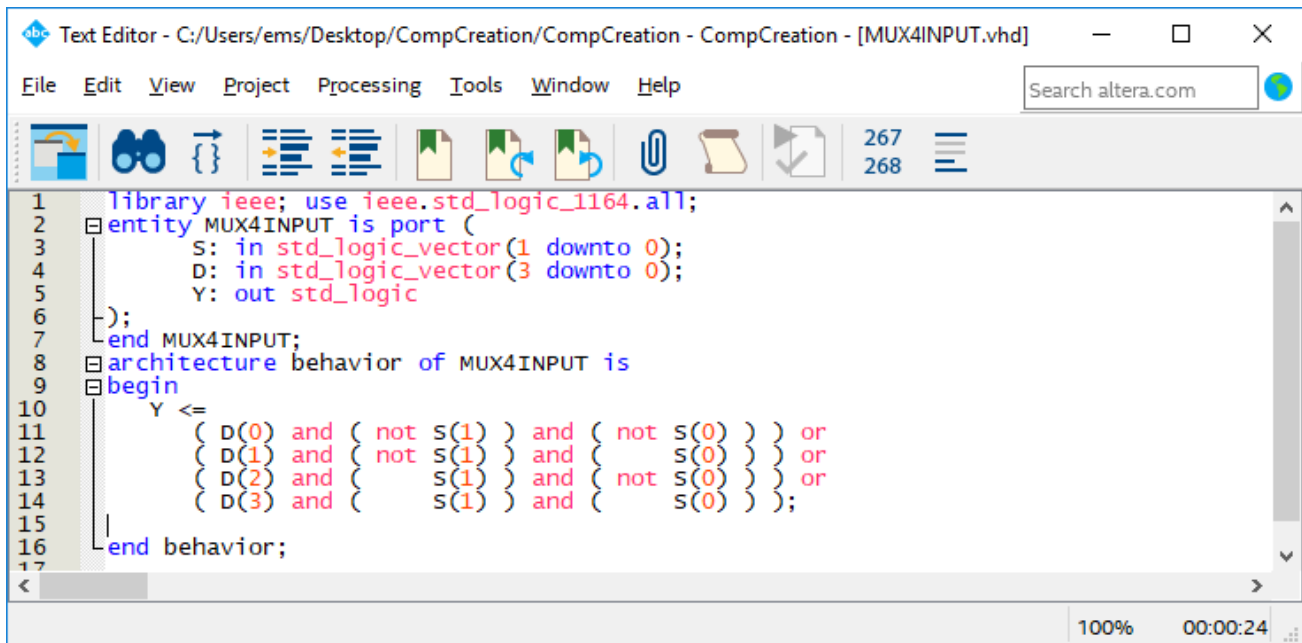
Question: How do I create a component from a previously designed schematic (BDF file), so that I can place it into a new schematic (BDF file)?

Answer: After successfully compiling the file, select the graphics editor window (BDF file) and then choose *File | Create / Update | Create Symbol Files for Current File*. This will create a file with the extension *bsf* in the same directory. This symbol can now be used in a new schematic.

Question: How do I create a component from previously designed VHDL code, so that I can place it into a new schematic (BDF file)?

Answer: After successfully compiling the file, select the VHDL file and then choose *File | Create / Update | Create Symbol Files for Current File*. This will create a file with the extension *bsf* in the same folder. This symbol can now be used in a new schematic. The below example will demonstrate the technique.

We would like to create a graphical component out of the MUX_4INPUT VHDL code shown below (MUX_4INPUT.vhd) and use it graphically in another design. (Alternatively, you could create this same MUX with several ANDs, ORs and NOTs using schematic entry in a BDF file.) Figure 1 shows an example VHDL file.



```
1 library ieee; use ieee.std_logic_1164.all;
2 entity MUX4INPUT is port (
3     S: in std_logic_vector(1 downto 0);
4     D: in std_logic_vector(3 downto 0);
5     Y: out std_logic
6 );
7 end MUX4INPUT;
8 architecture behavior of MUX4INPUT is
9 begin
10     Y <=
11         ( D(0) and ( not S(1) ) and ( not S(0) ) ) or
12         ( D(1) and ( not S(1) ) and ( not S(0) ) ) or
13         ( D(2) and ( not S(1) ) and ( not S(0) ) ) or
14         ( D(3) and ( not S(1) ) and ( not S(0) ) );
15 end behavior;
```

Figure 1: VHDL file.

The steps to create a graphical component for MUX_4INPUT.vhd (or a bdf file):

1. In Quartus, create a new project called CompCreation. I made the project CompCreation in folder CompCreation (for component creation). Create a vhd (or bdf file) called MUX4INPUT.vhd. Set this file as your “Top-Level Entity”, i.e., *Project | Set as Top-Level Entity* and then compile.
2. After compilation, select the design file (MUX4INPUT.vhd). Create a new symbol for this file by selecting *File | Create / Update | Create Symbol Files for Current File*. This will create a symbol file (MUX4INPUT.bsf) in the same folder.

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3. Create a new schematic entry (bdf) file in the same folder. This is the file in which you want to place your newly created VHDL (or schematic entry) component symbol. Now double-click the left mouse button to enter a symbol and select the symbol you just created (MUX_41a), as shown in this figure.

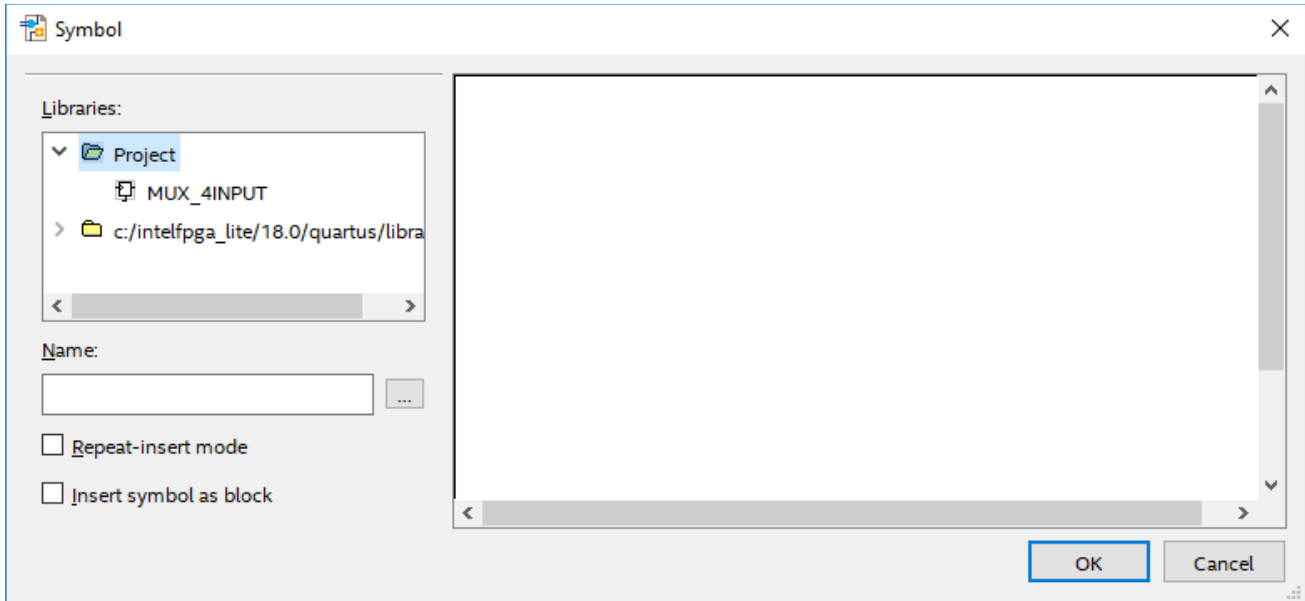


Figure 2: Insert symbol into schematic entry (bdf) file

4. Your schematic entry (bdf) file should look similar to Figure 3. Now save this file as CompCreation.bdf.

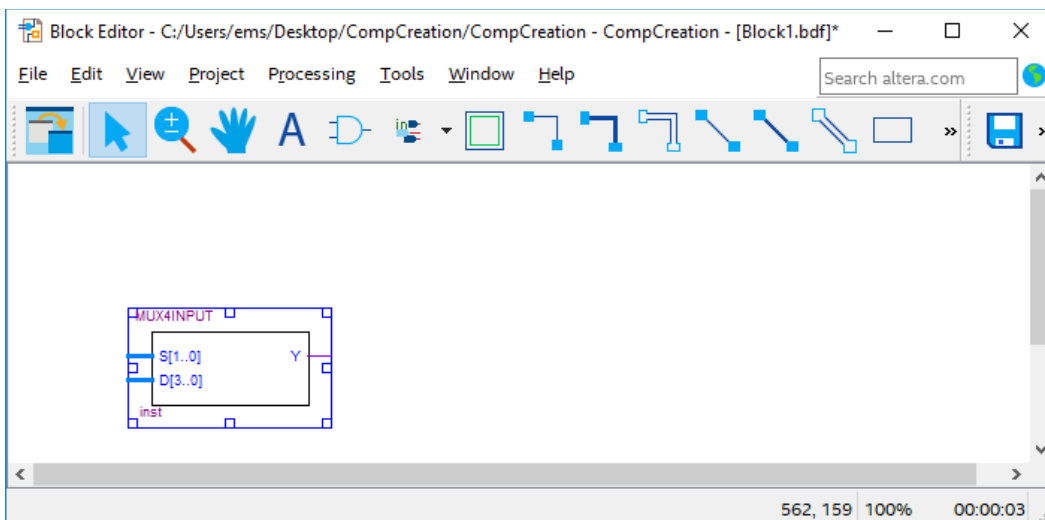


Figure 3: New MUX_4INPUT symbol inserted into new schematic entry (bdf) file

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5. You can now add wires & I/O to the component as you would any other component selected out of Altera's libraries, as shown in the figure below. Make this the "Top Level Entity" by selecting *Project / Set as Top-Level Entity* (or Ctrl-Shift-J). Then compile the design of the schematic entry (bdf) file as normal.

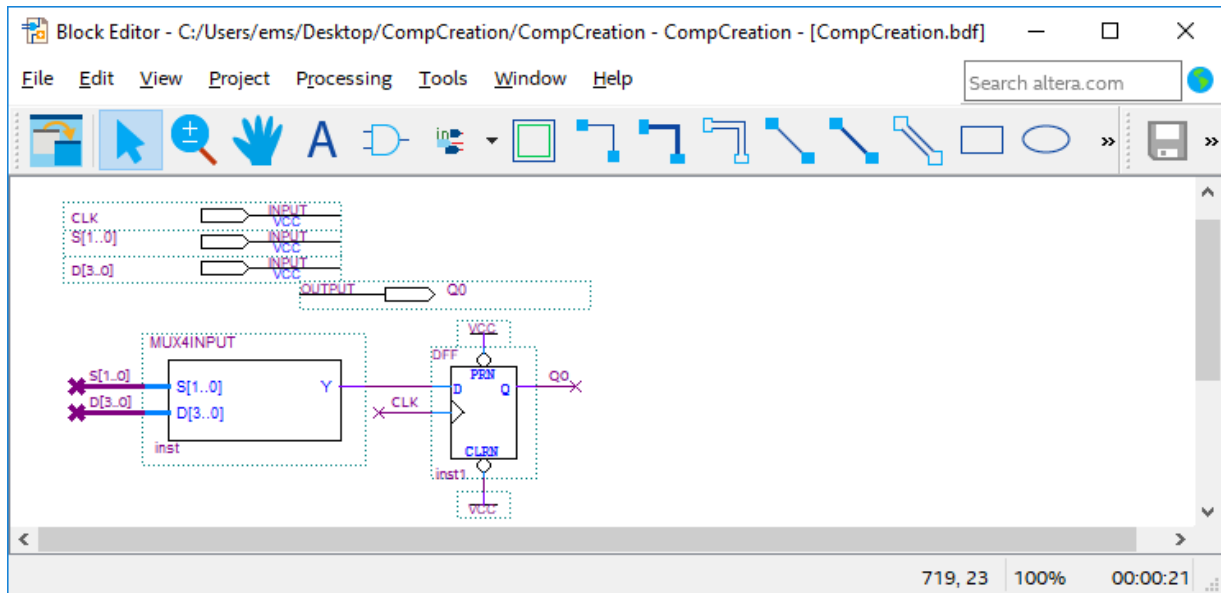


Figure 3: CompCreation.bdf file

Special Note: It is best not to name the VHDL component and BDF file the same name. Use different names for each.

Example application:

The logic equations for an ASM can be easily specified using VHDL, much more easily than graphically entering the gates in a schematic entry (bdf) file. More importantly, VHDL files can be changed easily during the debugging phase without having to redraw and connect the gates every time. Using the graphical symbol, the equations can then be integrated with the rest of the ASM.